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Engineering & Technology Services

Application Customized CPU Design for Microsoft XBOX 360™

Jeffrey D. Brown
Chief Engineer - Microsoft CPU Project
IBM Corporation

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CPU Chip Development Project Overview

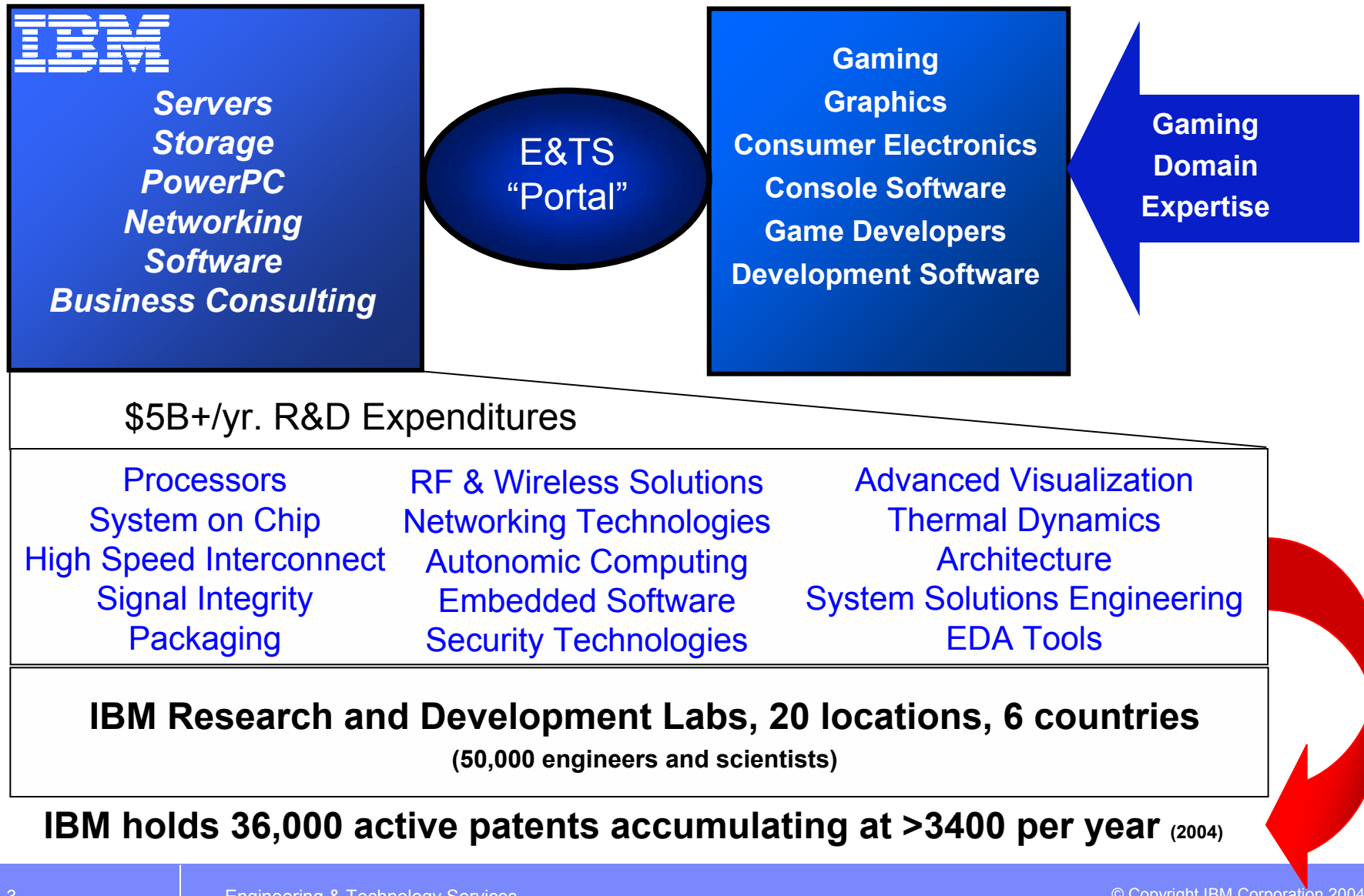
REDMOND, Wash., and EAST FISHKILL, N.Y. — Nov. 3, 2003 — *Microsoft Corp. today announced that it has entered into a semiconductor technology agreement with IBM Corp. Under the agreement, Microsoft has licensed leading-edge semiconductor processor technology from IBM for use in future Xbox® products and services to be announced at a later date.*

- CPU Chip for XBOX 360™ Console

- Hardware Solution Architected to match XBOX 360™ System Vision
 - Personalized System Architecture
 - Engineered solution optimized to consumer product constraints
 - Bridged from established design foundations to provide a spring board for development

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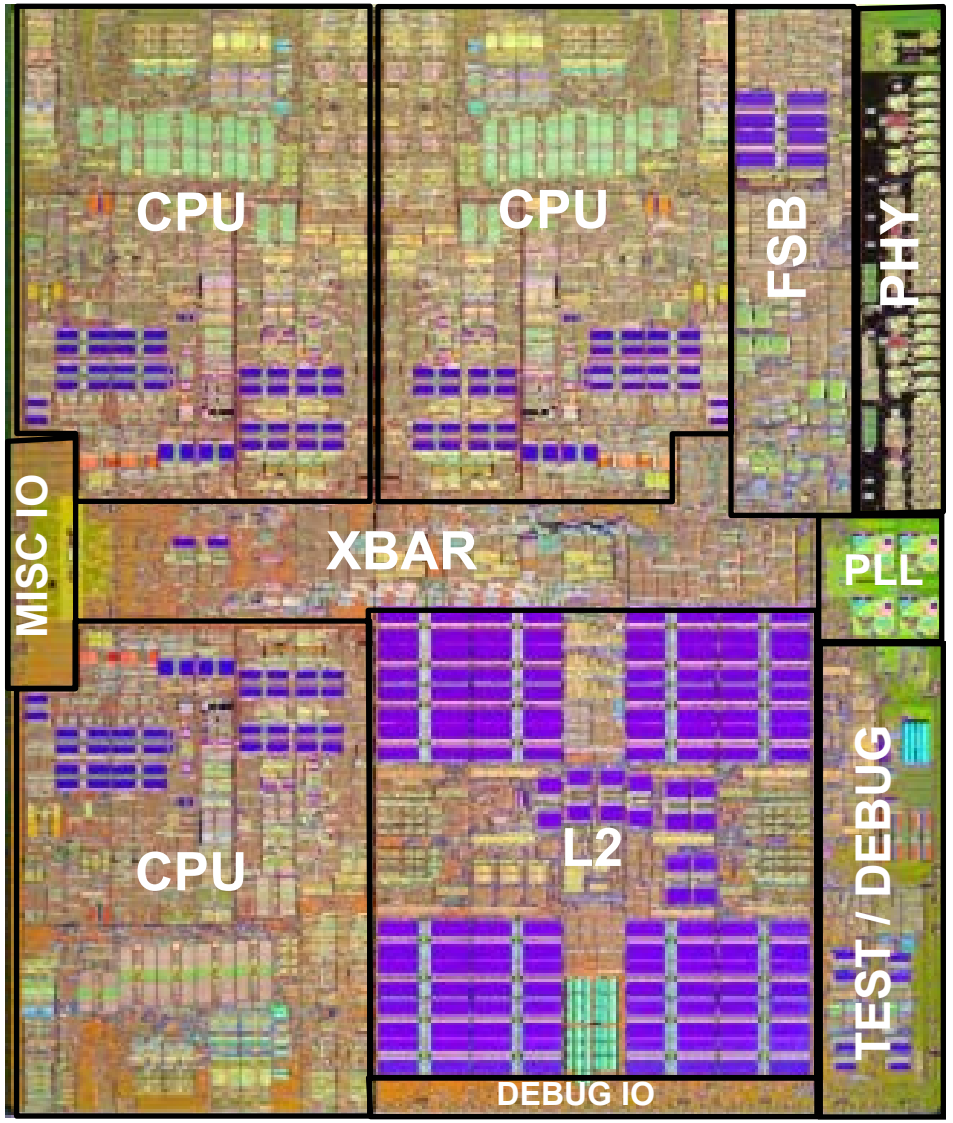
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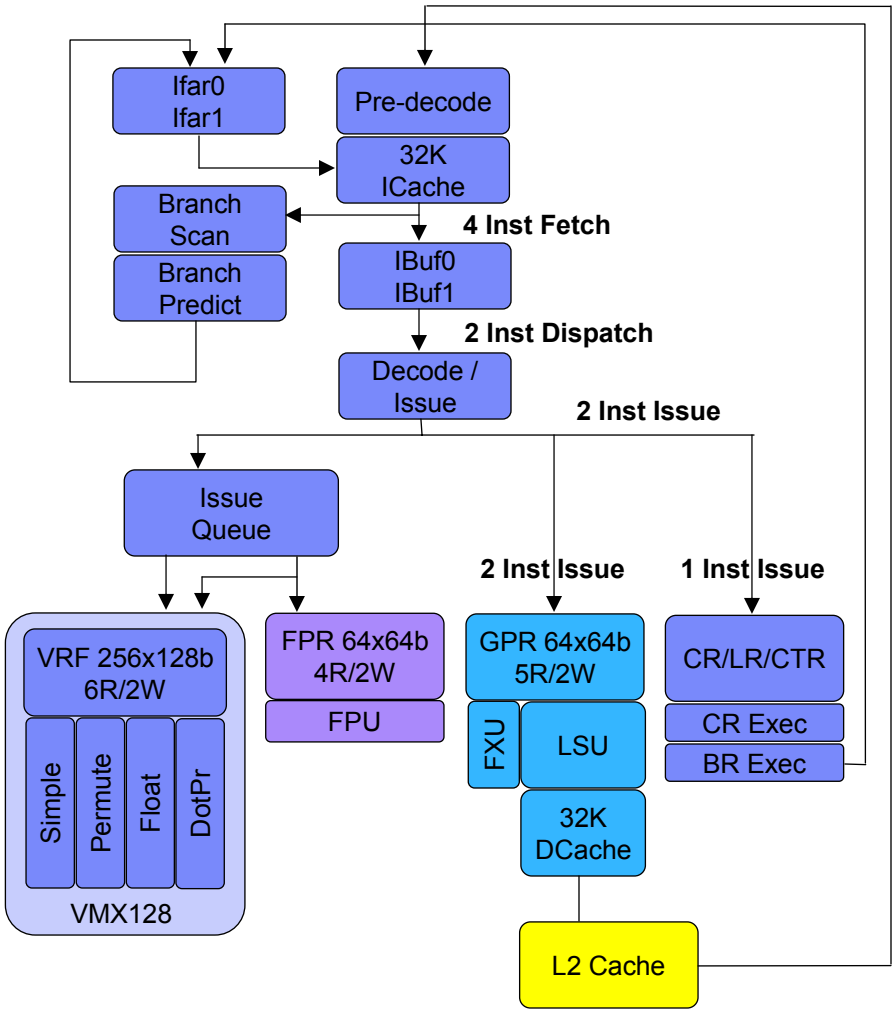
Xbox 360™ CPU Chip Overview

- 3-Way Symmetric Multi-Processor
 - IBM PowerPC Architecture®
 - Specialized Function VMX
 - 3.2GHz
- Shared 1 MByte L2
- Front Side Bus / PHY – 21.6 GB/sec
- Phase Locked Loops
 - 2 (if,hf) for core clocks
 - 2 (if,hf) for PHY clock
- Test/control functions
- Debug / Trace / performance monitor
- Manufacturing fuses
- redundancy, voltage, …
- MISC IO
 - JTAG, POST, VID, SPI
- 165 M Transistors
- IBM CMOS 10KE – 90nm SOI



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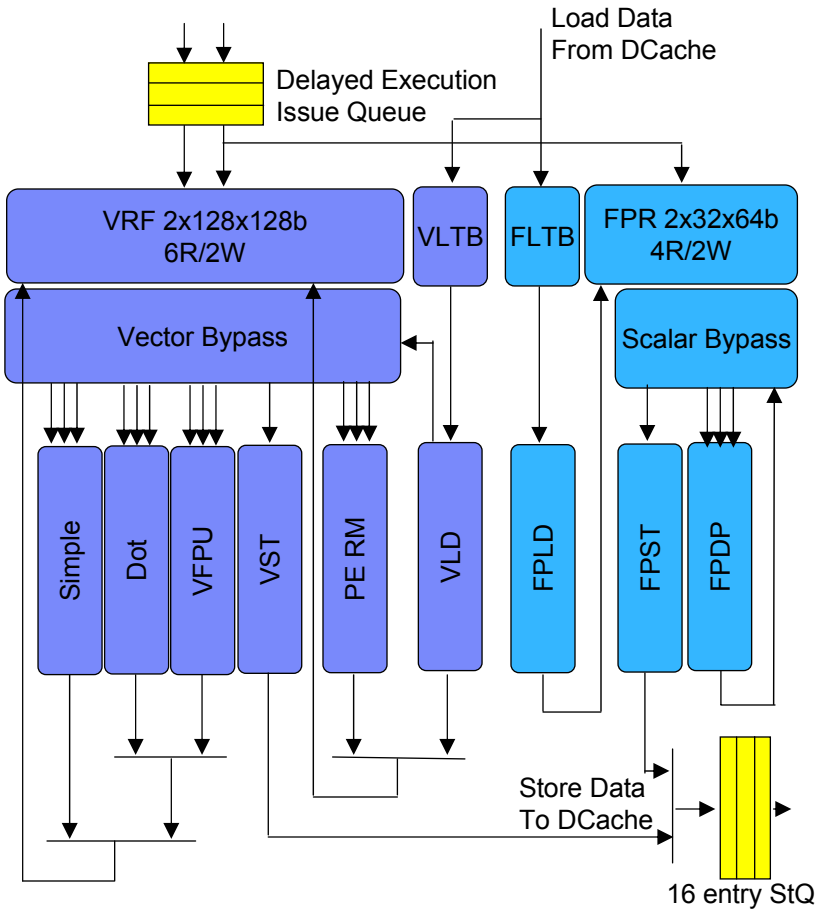
64b IBM PowerPC® -Architecture Core



- Highest Freq Power PC® ISA Core: 11 FO4
- Extensive Clock Gating for power efficiency
 - Pipelines shutdown until instruction active
- Instruction Unit
 - Multithreading – 2 simultaneous threads
 - ICache: 32KByte, 2 way, 128B line
 - 64 entry, 2 way, 1st level translation (ERAT)
 - 4Kx2 BHT per thread w/ Global Gshare
 - Two instruction In-Order Issue
 - Delayed execution to cover load use penalty
- Fixed Point and Load/Store execution
 - 2 FXU units – Simple / Complex
 - 2 cycle ALU op latency
 - 2 cycle fixed pt Ld latency - delayed execution
 - DCache
 - 32KByte, 4 way, 128 B line, store-thru
 - Non-blocking (hit under miss)
 - 64 entry, 2 way, 1st level translation (ERAT)
 - 1K, 4 way, 2nd level translation (TLB)
 - 8 entry MissQ, 16 entry StoreQ

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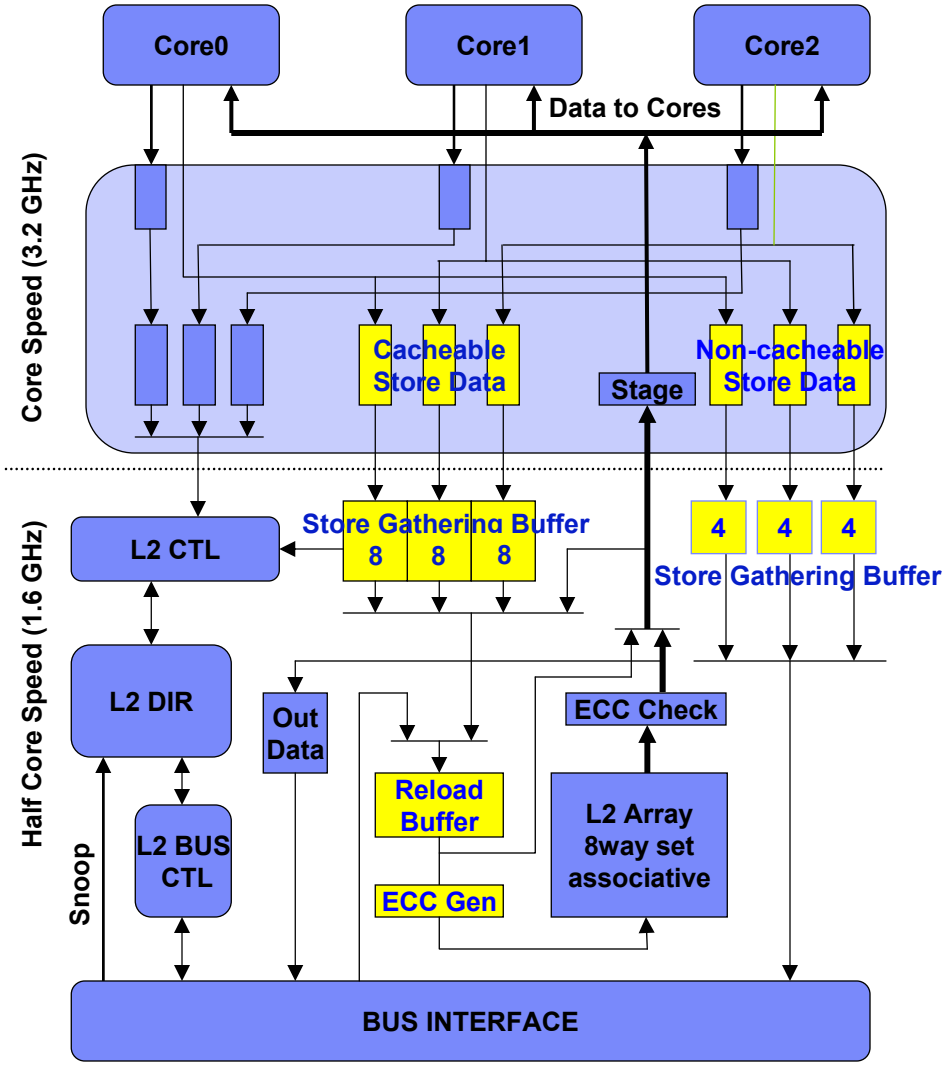
PowerPC® Core - Combined VMX and FPU Unit



- Extensive Clock Gating for power efficiency
- Instruction Sequencing
 - 2 simultaneous threads for both VMX and FPU
 - Delayed execution issue queue reduces VMX/FPU load latency to 2 cycles
 - Separate Load target buffer for VMX and FPU loads
 - LSU may execute out-of-order with respect to VMX/FPU
 - Decoupled FPU stores
 - Allows Stores to issue before store data available
 - Data cache 16 entry store queue
- Pipeline (11FO4)
 - 10 cycle Scalar DP FPU latency
 - 2 cycle Load latency
 - 4 cycle VMX simple/permute latency
 - 14 cycle VMX dot product latency
- New VMX128 Vector ISA
 - Focus on accelerating 3D graphics and physics
 - Extends VMX from 32 to 128 Vector Registers
 - Floating-point dot-product instructions
 - Permute-class instructions for data management
 - Direct3D Pack and unpack instructions
 - Misaligned storage access instructions
 - Maintains binary compatibility w/subset of VMX

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Shared L2 Cache Features



Cacheable (I=0)

- Cache Size : 1MB
- MESI Protocol
- 8-way set associative
- Pseudo-LRU
- Store Gathering per Core
 - 8 non-sequential Buffers
- ECC in Data Array
- Dual Directories
- Parity in DIR Array

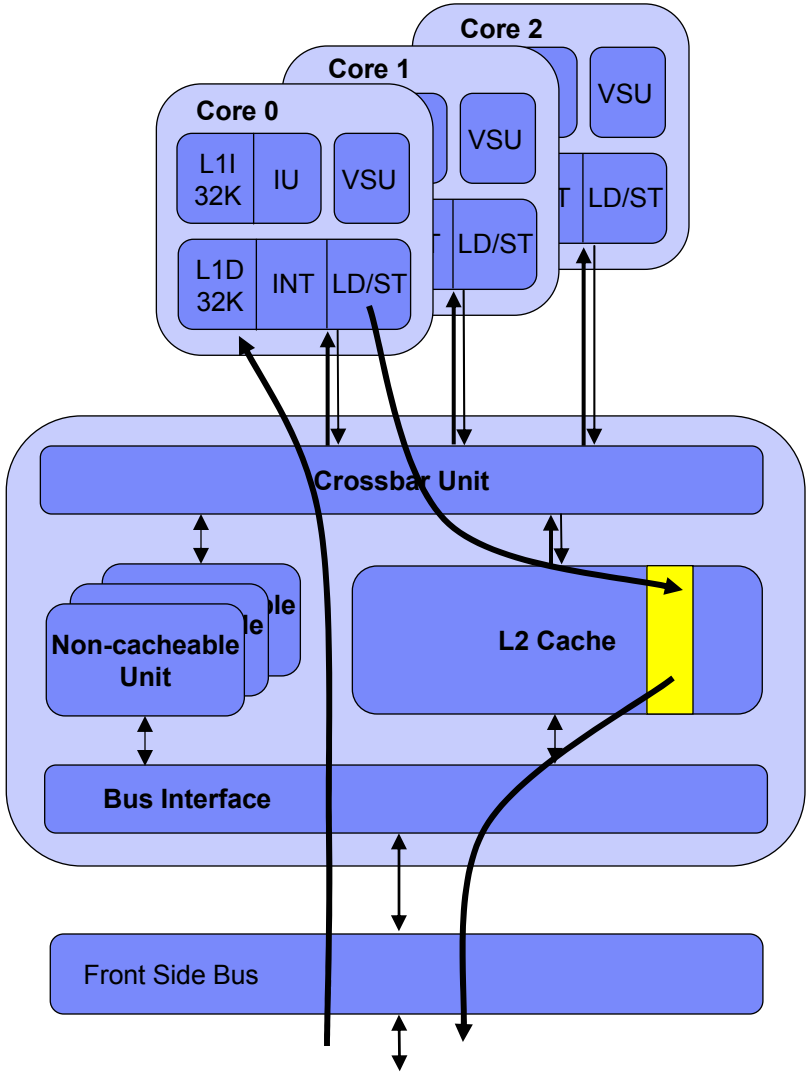
Cache Inhibited (I=1)

- Store Gathering per Core
 - 4 sequential Buffers
- Different Size Transfer

Support for High BW Streaming

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High Bandwidth Data Streaming Features



Read streaming

- xDCBT data prefetch around L2, directly into L1
- 8 outstanding load/prefetches per core

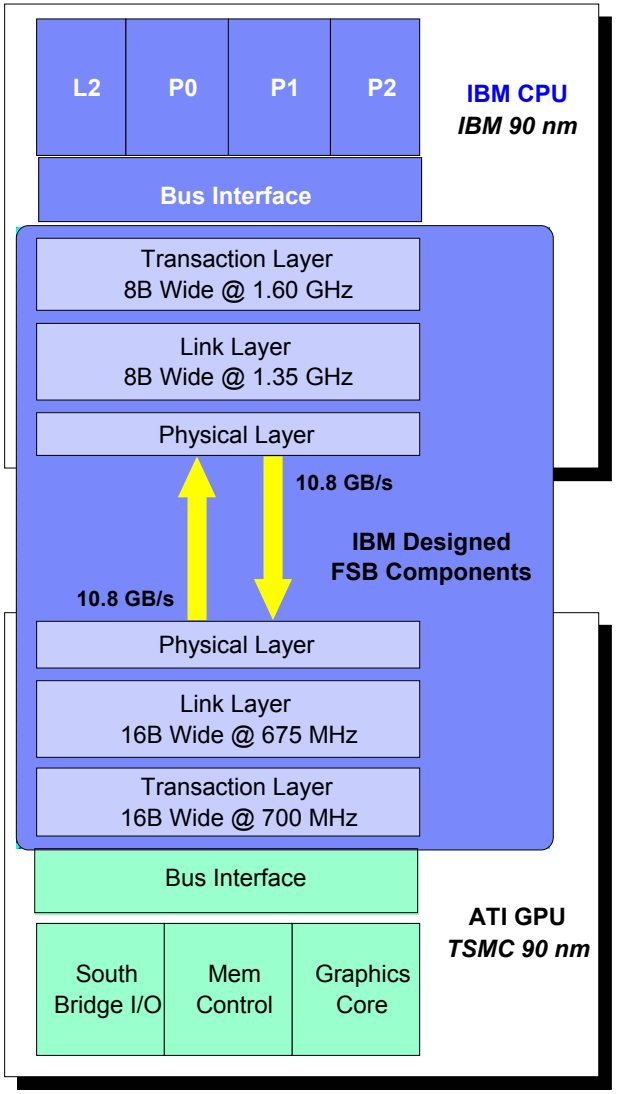
Write streaming

- L1s are write through, Writes do not allocate in L1
- Configurable L2 set locking for streaming buffers (avoids L2 thrashing)
- GPU 128B read from L2 (L2 retains ownership)

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Front Side Bus

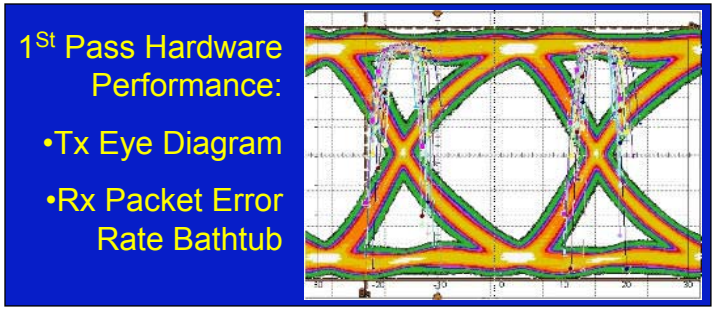
- FSB Architecture,
 - Architected and uniquely designed to meet throughput and latency requirements of the XBOX 360™ gaming platform
- FSB Unit
 - Common design for CPU and GPU
 - Asynchronous interface between FSB and Application domain
 - Automatic link initialization
 - Two Virtual Channels
- Transaction Layer
 - Common interface to application layer in CPU and GPU for transaction handling
 - Performs command reordering and tracking
- Link Layer
 - Accepts commands from transaction layer and builds FSB packets
 - Decodes FSB packets; performs consistency checks
 - Interfaces to FSB Physical Layer

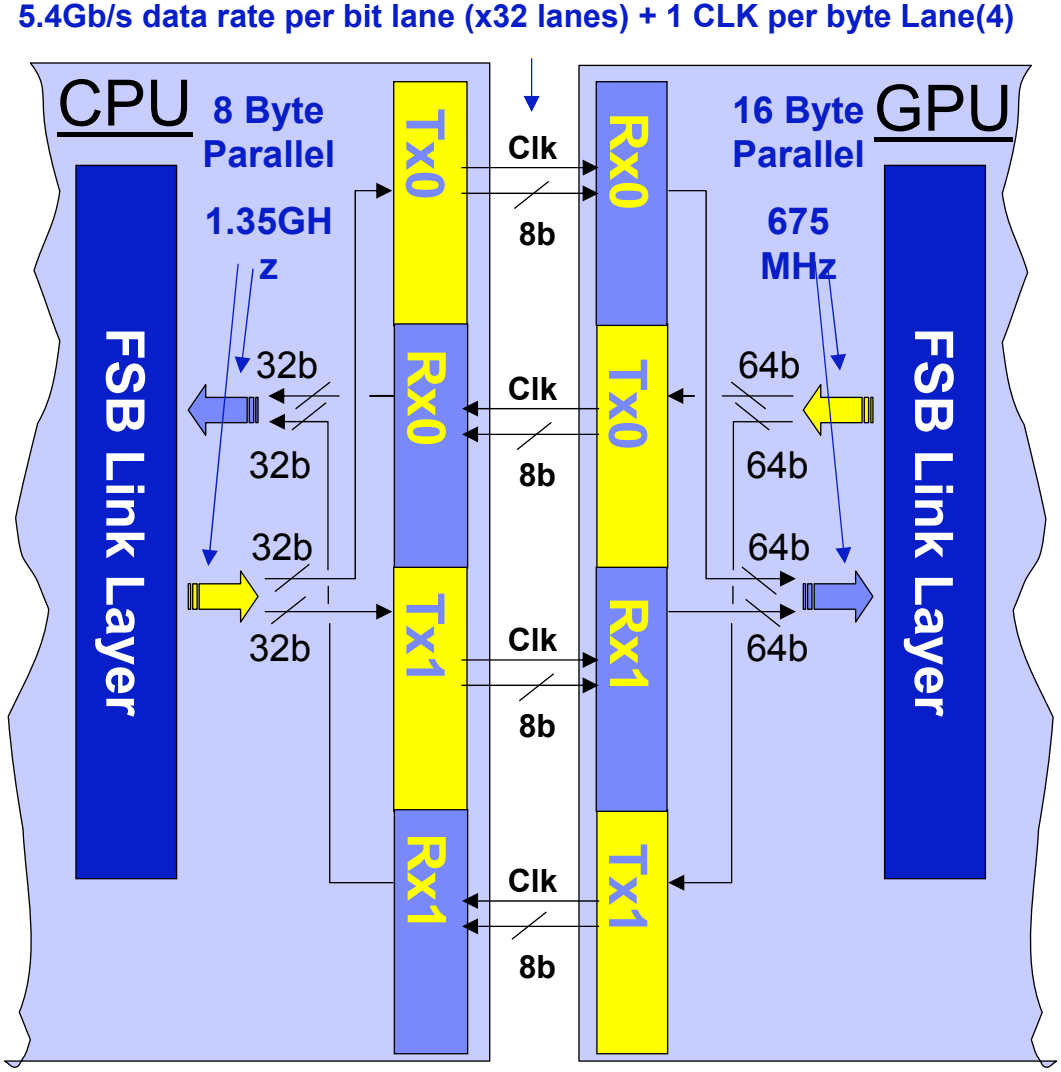


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Front Side Bus – Physical Layer

- 4:1 & 8:1, 5.4 Gb/s SerDes
 - Source Synchronous
 - 2 byte, full duplex operation
 - IBM SOI CMOS 10KE (CPU)
 - TSMC 90GT (GPU)
- 1.1V CML Based Design
 - Dynamic termination to 50 ohms
 - Low Jitter, High Noise Tolerance
- Low cost packaging
 - Organic Substrate
 - 2/2/2 on CPU
 - 3/2/3 on GPU
 - 2s, 2p System Card
 - 6 inches of wire

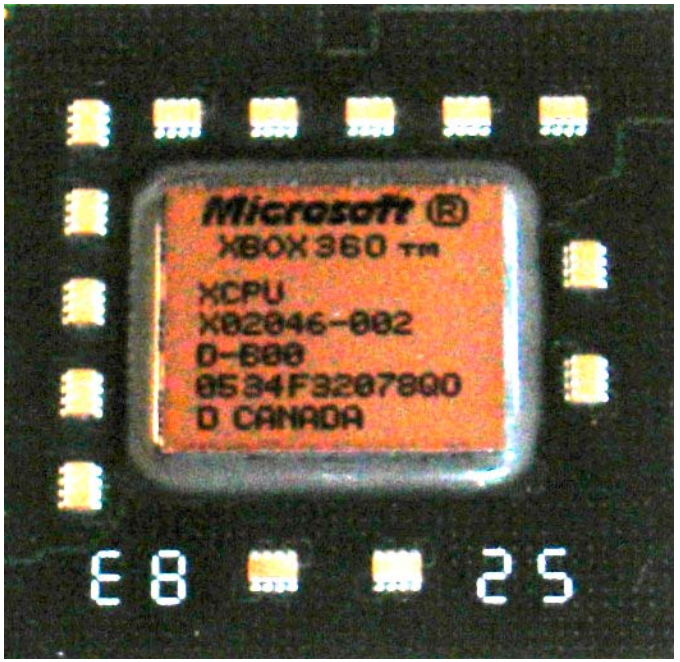




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Package Design

- Design Goal
 - High Volume Consumer Electronics Application
 - High Performance CPU Chip
- Package Definition
 - 2-2-2 FC-PBGA
 - 31mm x 31mm (1mm Pitch)
 - 800um Core Thickness, 20/20um Line Widths/Spaces
 - Supports 2s,2p system card
- Front Side Bus (5.4Gb/s Channel)
 - Differential Attenuation – 1.7dB @ fBaud/2
 - Return Loss - -10dB @ 0.75 * fBaud
 - Pair-to-Pair Isolation - -30dB @ 0.75*fBaud
- Power Distribution
 - (14) 100nF IDC Decoupling Capacitors
 - Lateral Leff (TSM to IDC) – 10pH
 - Vertical Leff (TSM to BSM) – 10pH



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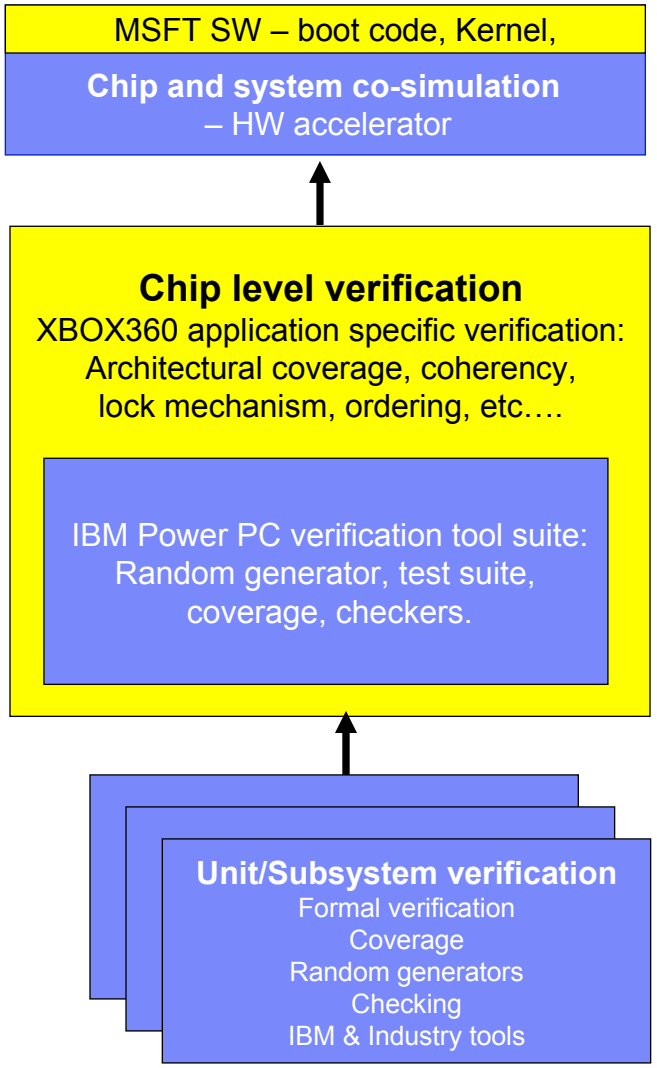
Test and Debug Features

- Test
 - AC Array BIST and AC Logic BIST @ full speed for maximum delay defect coverage
 - Functional “Ping” BIST @ full bus speed for Analog PHY coverage
 - All Scanning at tester speed limits to minimize tester time
 - 10 Test modes for Tester Flexibility
- Trace Arrays
 - 10 Local Trace Arrays @ full speed, 1000+ Internal signals traced
 - Robust local and global trigger & pattern matching capabilities
 - External Debug Bus for extended traces
 - 1 / 4 full speed for CPU
 - Full speed for FSB
- Performance Monitoring
 - 16 32-bit counters, 100s of events across all functional units
 - Programmable start/stop and synchronization conditions

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Design Validation

- First Time Right
 - Functional Pass 1 Hardware: Full speed Bus, Full speed CPU, Caches
 - Demo Game was running one week from power-on
- Verification Strategy
 - Parallel / Hierarchical verification
 - Focus on quality.
 - Quality measurement standards
 - Extensive review process
 - IBM verification tools as well as industry tools.
 - Intelligent IBM Randomized test generation
 - IBM Power PC Uni and Multi Processor test suite
 - Formal Verification where appropriate
 - Hardware accelerators for software/hardware co-simulation
 - Chip and system level co-simulation -IBM and Microsoft
 - System Power On Reset
 - System Level Coherency,
 - Boot code (Boot ROM) and Kernel development and validation.
- Lab Bringup
 - Joint BU & Validation effort with the Customer
 - Multiple bringup sites within IBM & Customer
 - Used IBM & Customer bringup tools



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Summary

- CPU Chip Designed by IBM E&TS for Microsoft's next generation gaming system
 - IBM E&TS website http://www-03.ibm.com/chips/
- Engineered solution optimized to consumer product constraints
- Delivered on schedule with quality



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Glossary

BHT	Branch History Table
BR	Branch Register
BSM	Bottom Side of Module
CR	Condition Register
CTR	Count Register
E&TS	Engineering & Technology Services
ECC	Error Correction Code
EDA	Engineering Design Automation
ERAT	Effective to Real Address Translation
FO4	Fan-Out of Four
FPDP	Floating Point Double Precision
FPLD	Floating Point Load
FPST	Floating Point Store
FPU	Floating Point Unit
FSB	Front Side Bus
FXU	Fixed Point Unit
GPR	General Purpose Register
GPU	Graphics Processing Unit
IDC	Interdigitated Capacitor
IFAR	Instruction Fetch Address Register
ISA	Instruction Set Architecture
LR	Link Register
LSU	Load Store Unit
MESI	Modified Exclusive Shared Invalid
PERM	Permute
PHY	Physical Layer
POST	Power On Self Test
SOI	Silicon On Insulator
SPI	Serial Peripheral Interface
TLB	Translate Look-aside Buffer
TSM	Top Side of Module
VFPU	Vector Floating Point Unit
VID	Voltage Identifier
VLD	Vector Load
VMX	Vector/SIMD Multimedia eXtension
VRF	Vector Register File
VST	Vector Store
XBAR	Cross Bar
xDCBT	extended Data Cache Block Touch

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